We Claim:

1. An electronic device, comprising:

a semiconductor chip having an active top side with a plurality of contact areas;

said semiconductor chip having a plurality of metallization layers and a plurality of insulation layers configured alternately one above another on said active top side;

said plurality of metallization layers having a plurality of voltage supply structures and/or a plurality of signal line structures;

said plurality of insulation layers formed with a plurality of passage contacts connecting said plurality of voltage supply structures and/or said plurality of signal line structures to said plurality of contact areas of said active top side;

said plurality of metallization layers including topmost metallization layers having area-covering ones of said plurality of voltage supply structures;

said topmost metallization layers having ones of said plurality of passage contacts connected to said plurality of contact areas;

said topmost metallization layers having at least a first one of said plurality of voltage supply structures for a low supply potential and a second one of said plurality of voltage supply structures for a high supply potential;

said first one of said plurality of voltage supply structures being insulated from said second one of said plurality of voltage supply structures;

ones of said plurality of metallization layers, being configured underneath said topmost metallization layers, having ones of said plurality of signal line structures;

said first one of said plurality of voltage supply structures of said topmost metallization layers having a grid of supply interconnects configured parallel to one another;

said second one of said plurality of voltage supply structures of said topmost metallization layers having a grid of supply interconnects configured parallel to one another; and

said grid of said first one of said plurality of voltage supply structures being rotated relative to said grid of said second one of said plurality of voltage supply structures.

2. The electronic device according to claim 1, wherein:

said semiconductor chip includes an integrated circuit subdivided into a plurality of functional module regions; and

each one of said plurality of module regions has a plurality of passage contacts connecting ones of said plurality of contact areas to said first one of said plurality of voltage supply structures and to said second one of said plurality of voltage supply structures.

3. The electronic device according to claim 1, wherein:

said semiconductor chip has a silicon chip made of monocrystalline material and has an integrated circuit near said active top side;

said integrated circuit has said plurality of contact areas and a plurality of interconnects configured above said plurality of contact areas;

said plurality of interconnects of said integrated circuit and said plurality of contact areas have electrical connections therebetween;

said electrical connections are effected via said plurality of passage contacts of said plurality of insulation layers; and

said electrical connections are wired automatically using place-route programs.

4. The electronic device according to claim 1, wherein:

said supply interconnects of said grid of said first one of said plurality of voltage supply structures alternately have different electrical supply potentials; and

said supply interconnects of said grid of said second one of said plurality of voltage supply structures alternately have different electrical supply potentials.

5. The electronic device according to claim 4, wherein:

said supply interconnects of said grid of said first one of said plurality of voltage supply structures are spaced apart at distances dimensioned to provide an electrical capacitance that is as high as possible with sufficient dielectric strength; and

said supply interconnects of said grid of said second one of said plurality of voltage supply structures are spaced apart

at distances dimensioned to provide an electrical capacitance that is as high as possible with sufficient dielectric strength.

6. The electronic device according to claim 1, wherein:

said supply interconnects of said grid of said first one of said plurality of voltage supply structures all have a first electrical supply potential; and

said supply interconnects of said grid of said second one of said plurality of voltage supply structures all have a second electrical supply potential that is different from said first electrical supply potential.

7. The electronic device according to claim 1, wherein ones of said plurality of insulation layers located between said topmost metallization layers have a thickness dimensioned to provide an electrical capacitance that is as high as possible with sufficient dielectric strength at areas of said topmost metallization layers that are configured one above another.

8. The electronic device according to claim 1, wherein said plurality of metallization layers include polycrystalline silicon, copper, aluminum, nickel, an alloy of copper, an alloy of aluminum, or an alloy of nickel.

9. The electronic device according to claim 1, wherein said plurality of insulation layers include silicon dioxide, silicon nitride, or polymeric plastics.

10. The electronic device according to claim 1, wherein:

said plurality of signal line structures have interconnects with a thickness and a width;

said supply interconnects of said grid of said first one of said plurality of voltage supply structures have a thickness and a width that are greater than said thickness and said width of said interconnects of said plurality of signal line structures; and

said supply interconnects of said grid of said second one of said plurality of voltage supply structures have a thickness and a width that are greater than said thickness and said width of said interconnects of said plurality of signal line structures.

11. A semiconductor wafer, comprising:

an active top side having a plurality of contact areas;

a plurality of semiconductor chip positions configured in rows and columns on said active top side;

each one of said plurality of semiconductor chip positions having a plurality of patterned metallization layers and a plurality of insulation layers configured alternately one above another, said plurality of insulation layers having a plurality of passage contacts, said plurality of metallization layers having a plurality of voltage supply structures and/or a plurality of signal line structures, said plurality of passage contacts configured in said insulation layers connecting said plurality of voltage supply structures and/or said plurality of signal line structures of said metallization layers to said plurality of contact areas on said active top side;

in each one of said plurality of semiconductor chip positions, said plurality of metallization layers including topmost metallization layers having area-covering ones of said plurality of voltage supply structures;

in each one of said plurality of semiconductor chip positions, said topmost metallization layers having at least a first one of said plurality of voltage supply structures for a low supply potential and a second one of said plurality of voltage supply structures for a high supply potential, said

first one of said plurality of voltage supply structures being insulated from said second one of said plurality of voltage supply structures;

each one of said plurality of semiconductor chip positions including a contact wire layer and a plurality of module regions configured below said topmost metallization layers;

in each one of said plurality of semiconductor chip positions, said topmost metallization layers having a plurality of passage contacts for electrically connecting said first one of said plurality of voltage supply structures and said second one of said plurality of voltage supply structures to said plurality of module regions via said contact wire layer;

in each one of said plurality of semiconductor chip positions, ones of said plurality of metallization layers, being configured underneath said topmost metallization layers, having ones of said plurality of signal line structures;

in each one of said plurality of semiconductor chip positions, said first one of said plurality of voltage supply structures of said topmost metallization layers having a grid of supply interconnects configured parallel to one another;

in each one of said plurality of semiconductor chip positions, said second one of said plurality of voltage supply structures of said topmost metallization layers having a grid of supply interconnects configured parallel to one another; and

in each one of said plurality of semiconductor chip positions, said grid of said first one of said plurality of voltage supply structures being rotated relative to said grid of said second one of said plurality of voltage supply structures.

12. The wafer according to claim 11, wherein:

each one of said plurality of semiconductor chip positions includes an integrated circuit subdivided into a plurality of functional module regions; and

each one of said plurality of module regions has a plurality of passage contacts connecting ones of said plurality of contact areas to said first one of said plurality of voltage supply structures and to said second one of said plurality of voltage supply structures in said one of said plurality of module regions.

13. The wafer according to claim 11, further comprising:

a silicon chip made of monocrystalline material; and

an integrated circuit near said active top side;

said integrated circuit having ones of said plurality of contact areas and a plurality of interconnects configured above said ones of said plurality of contact areas of said integrated circuit;

said plurality of interconnects of said integrated circuit and said ones of said plurality of contact areas of said integrated circuit having electrical connections therebetween;

said electrical connections effected via said plurality of passage contacts of said plurality of insulation layers; and

said electrical connections being wired automatically using place-route programs.

14. The wafer according to claim 11, wherein:

said supply interconnects of said grid of said first one of said plurality of voltage supply structures alternately have different electrical supply potentials; and

said supply interconnects of said grid of said second one of said plurality of voltage supply structures alternately have different electrical supply potentials.

15. The wafer according to claim 14, wherein:

said supply interconnects of said grid of said first one of said plurality of voltage supply structures are spaced apart at distances dimensioned to provide an electrical capacitance that is as high as possible with sufficient dielectric strength; and

said supply interconnects of said grid of said second one of said plurality of voltage supply structures are spaced apart at distances dimensioned to provide an electrical capacitance that is as high as possible with sufficient dielectric strength.

16. The wafer according to claim 11, wherein:

said supply interconnects of said grid of said first one of said plurality of voltage supply structures all have a first electrical supply potential; and

said supply interconnects of said grid of said second one of said plurality of voltage supply structures all have a second

electrical supply potential that is different from said first electrical supply potential.

17. The wafer according to claim 11, wherein ones of said plurality of insulation layers located between said topmost metallization layers have a thickness dimensioned to provide an electrical capacitance that is as high as possible with sufficient dielectric strength at areas of said topmost metallization layers that are configured one above another.

18. A method for producing a semiconductor wafer, which comprises:

providing the semiconductor wafer with a plurality of semiconductor chip positions, a plurality of metallization layers having signal line structures, and a plurality of insulation layers configured in between said plurality of said metallization layers, the plurality of insulation layers having passage contacts, the signal line structures connected via the passage contacts to contact areas on an active top side of the semiconductor wafer;

applying a closed metallization layer to a topmost insulation layer of the signal line structures;

using a place-route program to automatically design positions of a grid of parallel supply interconnects serving as a first voltage supply structure and patterning the closed metallization layer to form the grid of the parallel supply interconnects;

using a place-route program to automatically design a photolithography mask;

applying an insulation layer to the first voltage supply structure and using the photolithography mask to set positions of passage contacts to the contact areas on the active top side;

using a place-route program to automatically design positions of a grid of parallel supply interconnects configured transversely to the first voltage supply structure;

applying and patterning a further metallization layer with the further grid of parallel supply interconnects configured transversely to the first voltage supply structure; and

applying a passivation layer such that contact pads, which are electrically connected to the passage contacts, are not covered by the passivation layer.

19. A method for producing a plurality of electronic devices, which comprises:

providing the semiconductor wafer produced by the method according to claim 18;

separating the semiconductor wafer into a plurality of semiconductor chips having contact pads;

applying the plurality of semiconductor chips to a leadframe with a plurality of device positions;

in each of the device positions, producing bonding connections between the leadframe and the contact pads of one of the plurality of semiconductor chips;

in each of the device positions, packaging one of the plurality of semiconductor chips in a plastic housing having external contacts; and

separating the leadframe into the plurality of electronic devices.